from the filling of a relatively wide trench which would require much thicker deposits because such a trench primarily would be filled in a direction upwards from the trench bottom.

Referring now to FIG. 2, a conformal coating 22 of a masking material is deposited upon the etched structure of FIG. 1 by a chemical vapor deposition method or by a plasma deposition method, so that the coating is deposited with uniform thickness on the horizontal as well as the vertical surfaces of the etched semiconductor body. The thickness of the deposited conformal coating 22 is selected to be equal to the width of each of a spaced succession of semiconductor mesas to be described later in connection with FIG. 4.

The coated semiconductor body is reactively ion etched to remove the conformal coating 22 from the horizontal body surfaces and to leave the coating 22 along only the vertical surfaces of the etched body as shown in FIG. 3. A suitable chemical-vapor-deposition process for depositing conformal coating 22 and a suitable reactive ion etching process for removing coating 22 from the horizontal body surfaces are described in copending patent application, Ser. No. 957,604, for "Method for Forming a Narrow Dimensioned Region on a Body", filed on Nov. 3, 1978, in the name of H. B. Pogge and assigned to the present assignee. As set forth in said copending patent application, it is important that the vertical surfaces 18 of the etched semiconductor body, as shown in FIG. 1, be substantially vertical (equal to or less than about 5 degrees from the vertical) so as to produce the desired result as shown in FIG. 3 subsequent to the reactive ion etching step. The conformal coating 22 may be composed of a variety of materials or combinations of materials which include silicon dioxide, silicon nitride, aluminum oxide, and the like. The reactive ion etching apparatus and process are further described in copending patent application, Ser. No. 594,413, filed July 9, 1975 in the name of J. N. Harvilchuck and in continuation patent application, Ser. No. 822,755 filed Aug. 8, 1977 and assigned to the present assignee. The reactive ion or plasma ambient in the Harvilchuck et al. patent application is reactive chlorine, bromine or iodine species, preferably a combination of the chlorine species with an inert gas such as argon. Application of suitable power in the order of about 0.1 to 0.50 watts/cm^2 from an RF voltage source will produce sufficient power density to cause the reactive ion etching operation of the conformal coating 22 to be carried out at a rate of about 0.01 to 0.5 micrometers per minute.

The desired result of the etching is shown in FIG. 3 wherein the conformal coating 22 is substantially or completely removed from the horizontal surfaces of the semiconductor body. There is substantially no effect on the coating 22 which is present on the vertical surfaces 18 of the trenches 16. The result is the narrow dimensioned regions 24 of the original conformal coating 22 as shown in FIG. 3.

The structure of FIG. 3 is reactively ion etched to the intended depth of the desired wide, deep recessed oxide isolation trenches, using the remaining conformal coating portions 24 as the etching mask. The result is shown in FIG. 4. It will be noted that all of the trenches penetrate into P$^-$ substrate 10.

As is well understood in the art, the formation of a P^{30} region underneath the dielectric material which will be used to fill the etched trenches of FIG. 4, may be desirable when the substrate is P$^-$ as is the case in the disclosed embodiment. The P$^-$ region has a tendency to change its resistivity, even to the extent of inverting to N-type material, when it is subjected to thermal oxidation. A P$^+$ implant in substrate 10 at the bottoms of the individual etched trenches prevents such inversion possibility. This may be formed by use of a P$^+$ ion implantation of a dopant such as boron. Accordingly, a thin silicon dioxide layer (not shown) is deposited on the structure of FIG. 4 to act as a screen for the aforesaid boron ion implantation and the ion implantation is carried out to produce the P$^+$ channel stops 26 shown in FIG. 5.

After the implantation step, the resulting structure is thermally oxidized to convert all of the silicon in the mesas 28 of FIG. 4 to silicon dioxide. The thermally grown silicon dioxide occupies regions 30 as shown in FIG. 5. At this point, there remain unfilled volumes 32 of trenches (adjacent the regions 30 of FIG. 5). The remaining unfilled trench portions 32 are filled by the chemical-vapor-deposition or plasma deposition of silicon dioxide or other dielectric material. The deposited dielectric material is removed from the surfaces of the semiconductor body corresponding to the device regions 34 by selective etching in a conventional manner. The wide, deep recessed isolation trench, filled with dielectric material as shown in FIG. 5, provides a structure for supporting signal carrying surface conductors (not shown) with minimum capacitive coupling to underlying substrate 10.

Having thus described our invention, what we claim as new, and desire to secure by Letters Patent is:

1. A method for making wide, deep recessed oxide isolation trenches in a semiconductor substrate comprising:
- forming a spaced succession of narrow, shallow trenches in said substrate, said shallow trenches having substantially vertical sidewalls and being saparated by semiconductor mesas,
- depositing a predetermined thickness of a masking material on the sidewall and on the bottom surfaces of said shallow trenches and on the top surfaces of said mesas,
- etching said coating to remove said coating substantially only from said bottom surfaces of said shallow trenches and from the top surfaces of said mesas,
- reactively ion etching said substrate using said coating on said sidewalls of said shallow trenches as a reactive ion etching mask to produce a spaced succession of narrow, deep trenches separated by narrow semiconductor mesas,
- the thickness of said narrow semiconductor mesas being substantially equal to and determined by the thickness of said coating, and
- thermally oxidizing said substrate so as to completely oxidize the semiconductor material of said narrow semiconductor mesas.

2. The method defined in claim 1 and further including the step of filling in any remaining spaces between said oxidized narrow semiconductor mesas by depositing a dielectric material.

3. The method defined in claim 2 wherein said dielectric material is chemical-vapor-deposited or plasma deposited silicon dioxide.

4. The method defined in claim 1 wherein said masking material is chemical-vapor-deposited or plasma deposited.